REMARKS/ARGUMENTS

This Amendment is submitted in response to the first Official Action dated March 23, 2005 in which objection was first made to the Abstract of the Disclosure as being too lengthy. The Abstract has been edited down to 144 words in accordance with the Examiner's instructions.

Concerning the rejection on the merits, claims 1-4 have been rejected under 35 U.S.C. §102 as being anticipated either by the Hembree et al. U.S. Patent 6,642,730 or by the Baba et al. U.S. Patent 5,969,426. These rejections are respectfully traversed.

It is well established that in order for a claim of a patent to be anticipated by a prior art reference, it is necessary that each of the claimed elements (or steps in the case of a process patent) be identically disclosed within the four corners of a single cited reference. Neither the Hembree et al. '730 nor the Baba et al. '426 patents satisfy this requirement.

Generally speaking, the Hembree et al. '730 patent teaches how to make a test fixture or carrier that constitutes a custom ball grid socket to be used to **temporarily** hold an uncased semiconductor component having bond pads or solder ball contacts that engage contacts on an interconnect that forms part of the test fixture. Also forming part of the test fixture is a base or substrate that has a plurality of terminal leads thereon. The terminal leads are wire-bonded to the interconnect contacts. The Hembree et al. arrangement teaches away from applicant's method where the uncased semiconductor die is **permanently** affixed to TAB tape and where wire bonds are used to connect the solder ball contacts on the uncased semiconductor die to bond pads on the TAB tape and where the uncased die and the wire bonds and the bond pads are then overmolded with plastic. In accordance with applicant's claimed method, only after the uncased die, the wire bonds and the bond pads on the TAB tape are overmolded with plastic does the test and burn-in step occur where the test pad contacts on the TAB tape are used as the input/output contacts. After the test and burn-in step, the TAB tape is severed to separate the test pad contacts from the portion of the TAB tape that is encapsulated along with the semiconductor die.

Further, in the Hembree et al. '730 teaching, the test fixture is reusable after the semiconductor has been tested and removed. In the method defined by claims 1 and 3 of the present invention, a portion of the TAB tape becomes an integral part of the now packaged and tested semiconductor chip.

Given the foregoing differences between the subject matter claimed and what is taught by the Hembree et al. reference, it cannot fairly be said that Hembree anticipates independent claims 1 and 3.

The same holds true for the Baba et al. '426 patent. It describes a method that is different in several respects from what is disclosed and claimed by applicant.

As set out in column 9, lines 54-61, that has been cited by the Examiner, test and burn-in are performed **prior to** encapsulation in fabricating the device of Figure 11 and not after as in applicant's claimed method. This fact is repeated at column 18, lines 8-11, of the Baba et al. reference. Also, there is no mention in the cited Baba et al. reference of singulating multiple packaged components by severing the tape on which a plurality of encapsulated components are affixed such that the portion of the TAB tape carrying the test pads is separated from the portion carrying the bond pads that is also encapsulated by the plastic used to overmold the semiconductor die.

The Baba et al. reference also does not teach or suggest a method starting with a commercially available TAB tape frame of a type having test pads, bond pads and ball grid array formed thereon as called for by step (a) of independent claims 1 and 3.

Applicant's attorney has amended the claims to better emphasis that the overmolding step is performed prior to the testing and burn-in step. As indicated above, just the opposite is true as regards Hembree et al and Baba et al.

It is, therefore, submitted that none of the claims, as now amended, is anticipated by one or the other of the Hembree et al. and Baba et al. patents. Moreover, given the differences between applicant's method of preparing an integrated circuit module and the methods involved in the Hembree et al. and Baba et al. patents, it cannot be said that applicant's method would have been obvious from the teachings of the cited references either when considered singly or in combination.

In that all of the claims remaining in the application are deemed to be in condition for allowance, a Notice to that effect is respectfully solicited.

Respectfully submitted,

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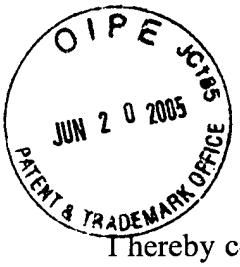

CERTIFICATE OF MAILING

I hereby certify that the foregoing Amendment is filed in response to the Official Action of March 23, 2005, in application Serial No. 10/782,5-5, filed on February 18, 2004, of James E. Blood, entitled "Method for Preparing Integrated Circuit Modules for Attachment to printed Circuit Substrates" is being deposited with the U.S. Postal Service as First Class mail in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, postage prepaid, on June 16, 2005.

Date of Signature: June 16, 2005.

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